IM6100 CMOS 12 Bit Microprocessor

FEATURES

- **Silicon Gate Complementary MOS**
- **Fully Static - 0 to 5.7 MHz**
- **Single Power Supply**
  - **IM6100 V_{CC} = 5 volts**
  - **IM6100A V_{CC} = 10 volts**
- **Crystal Controlled On Chip Timing**
- **PDP®-8/e, Instruction Set Compatible**
- **Low Power Dissipation**
  - **< 10mW @ 3.3 MHz @ 5 volts**
- **TTL Compatible at 5 volts**
- **Excellent Noise Immunity**
- **Direct Memory Access (DMA)**
- **Interrupt**

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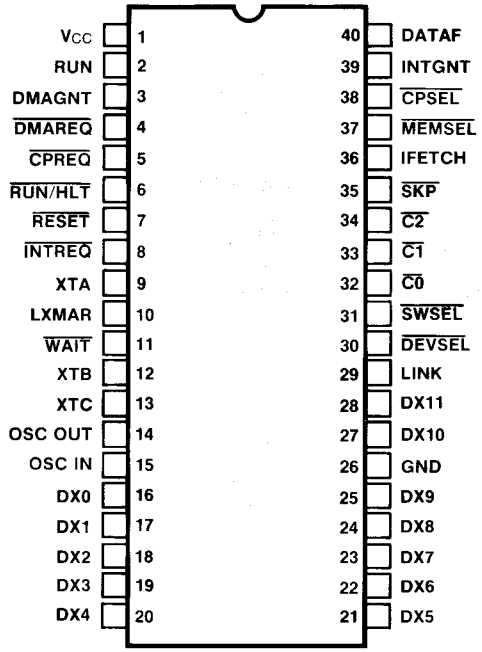
GENERAL DESCRIPTION

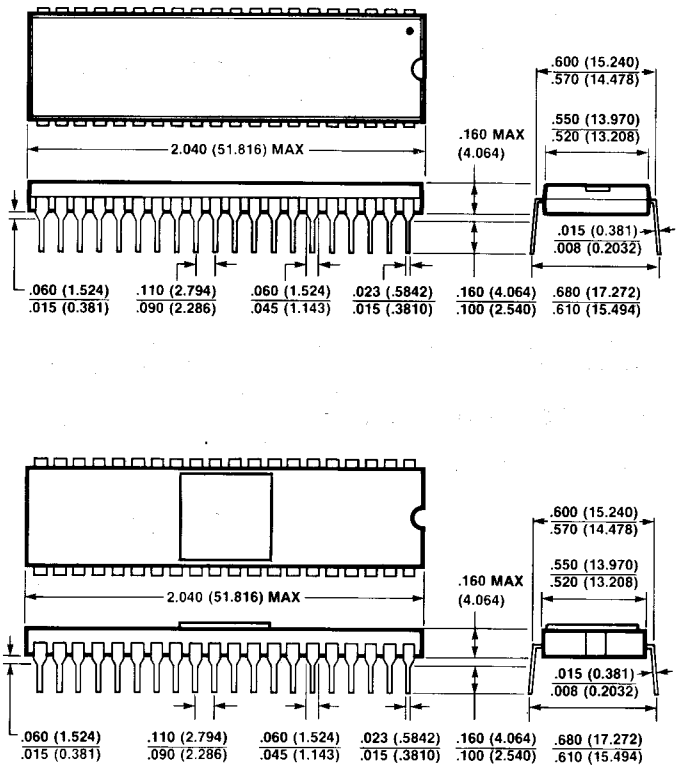
The IM6100 is a fixed word length, single word instruction, parallel transfer microprocessor using 12-bit, two's complement arithmetic which recognizes the instruction set of Digital Equipment Corporation's PDP-8/e minicomputer. The internal circuitry is completely static and designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal, thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

The IM6100 family includes IM6101 (Programmable Interfacing Element), IM6102 (Memory Extension/DMA Controller/Interval Timer), IM6103 (Parallel Input-Output Port), IM6512 (64 x 12 RAM), IM6312 (1k x 12 ROM), and IM6402/03 (UART), all featuring ultra low power-high noise immunity CMOS characteristics. The entire family is supported by the 6910 Intercept II Microcomputer Development System.

PIN CONFIGURATION



PACKAGE DIMENSIONS



ORDERING INFORMATION

ORDER CODE	IM6100-1	IM6100A	IM6100
PLASTIC PKG.	IM6100-1IPL	IM6100-AIPL	IM6100-IPL
CERAMIC PKG.	IM6100-1IDL	IM6100-AIDL	—
MILITARY TEMP.	IM6100-1MDL	IM6100-AMDL	—
MILITARY TEMP. WITH 883B	IM6100-1MDL/ 883B	IM6100-AMDL/ 883B	—

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