HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
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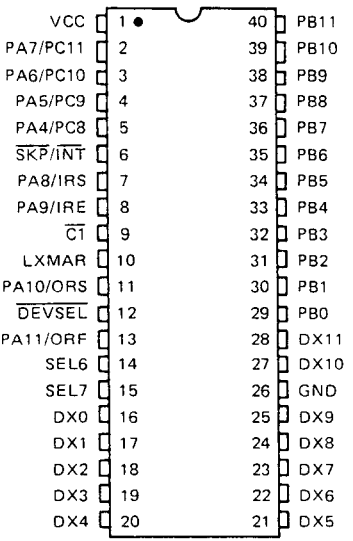
HD-6103

CMOS PARALLEL INPUT/OUTPUT PORT (PIO)

Features

- HM-6100 COMPATIBLE
- LOW POWER - TYP. $< 5.0\mu W$ STANDBY
- SINGLE SUPPLY 4-11 VOLT
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- IDEAL FOR MINIMUM SYSTEMS
- 20 PROGRAMMABLE BI-DIRECTIONAL I/O PINS
- THREE MODES OF OPERATION
- SOFTWARE POLLED INTERRUPTS
- UP TO 4 PIO'S PER SYSTEM
- 16 INSTRUCTIONS FOR PIO CONTROL

Pinout

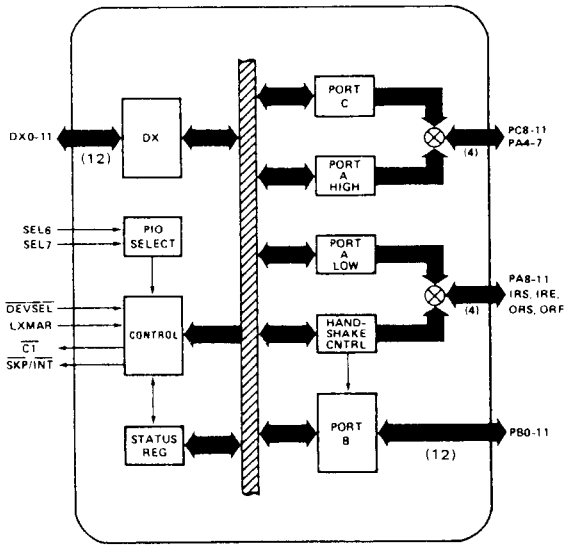


Description

The HD-6103 Parallel Input/Output Port (PIO) is a high speed, low power, silicon gate CMOS general purpose device which provides parallel data transfers and interrupt control for a variety of peripheral functions, such as displays, keyboards, A/D converters, etc. Data transfers between the HD-6103 are via Input/Output Transfer (IOT) instructions, control lines and DX bus. The PIO is ideal for minimum system configurations.

The HD-6103 has 20 I/O pins that are programmable in groups of 4, 8, or 12 bits via three modes of operation. In one mode, 4 of the pins are utilized as handshake control lines.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	Gnd. -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6103A-9	-40°C to +85°C
Military HD-6103A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 10.0 ± 0.5% Volts, TA = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	1.0		1.0	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt. (1)	VCC-2.0			V	IOH = -0.2mA
VOL	Logical "0" Output Voltage			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		1.0	μA	$0V \leq VO \leq VCC$
ICC	Supply Current (static)		1.0	800	μA	VIN = VCC, Freq. = 0
CI	Input Capacitance (2)		5	7	pF	
CO	Output Capacitance (2)		8	10	pF	
CIO	Input/Output Capacitance (2)		8	10	pF	

Notes: (1) Except pins 6, 9
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 10V			
SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
tLX	LXMAR Pulse Width	100		ns	CL = 50pF
tAS	Address Set-Up Time	20		ns	See Timing Diagram
tAH	Address Hold Time	40		ns	
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$		80	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		90	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		100	ns	
tDS	Data Setup Time	10		ns	
tDH	Data Hold Time	50		ns	
tDPO	Delay: $\overline{DEVSEL}$ to Port Data		10	ns	
tPSLX	Port Data Setup LXMAR	10		ns	
tPHLX	Port Data Hold LXMAR	50		ns	
tPSIR	Port Data Setup IRS	5		ns	
tPHIR	Port Data Hold IRS	50		ns	
tPEN	Port B Enable Time		75	ns	
tPDIS	Port B Disable Time		75	ns	
tDR	Delay: IRS to IRE				
	ORS to ORF				
	$\overline{DEVSEL}$ to IRE				
	$\overline{DEVSEL}$ to ORF		150	ns	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	Gnd. -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6103-9	-40°C to +85°C
Military HD-6103-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 10% Volts, TA = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-1.0		1.0	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt.(1)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Voltage			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		1.0	μA	$0V \leq VO \leq VCC$
ICC	Supply Current (static)		1.0	100	μA	VIN = VCC, Freq. = 0
CI	Input Capacitance (2)		5	7	pF	
CO	Output Capacitance (2)		8	10	pF	
CIO	Input/Output Capacitance (2)		8	10	pF	

Notes: (1) Except pins 6, 9
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 5.0V			
SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
tLX	LXMAR Pulse Width	200		ns	CL = 50pF
tAS	Address Setup Time	40		ns	See Timing Diagram
tAH	Address Hold Time	80		ns	
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$ $\overline{C2}$		160	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		180	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		200	ns	
tDS	Data Setup Time	20		ns	
tDH	Data Hold Time	100		ns	
tDPO	Delay: $\overline{DEVSEL}$ to Port Data		20	ns	
tPSLX	Port Data Setup LXMAR	20		ns	
tPHLX	Port Data Hold LXMAR	100		ns	
tPSIR	Port Data Setup IRS	10		ns	
tPHIR	Port Data Hold IRS	100		ns	
tPEN	Port B Enable Time		150	ns	
tPDIS	Port B Disable Time		150	ns	
tDR	Delay: IRS to IRE				
	ORS to ORF				
	$\overline{DEVSEL}$ to IRE				
	$\overline{DEVSEL}$ to ORF		300	ns	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	Gnd. -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6103C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 5% Volts, TA = Industrial

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			.8	V	
IIL	Input Leakage	-10		+10	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Volt.(1)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Voltage			0.45	V	IOL = 1.6mA
IO	Output Leakage	-10		+10	μA	0V ≤ VO ≤ VCC
ICC	Supply Current (static)		1.0	500	μA	VIN = VCC, Freq. = 0
CI	Input Capacitance (2)		5	7	pF	
CO	Output Capacitance (2)		8	10	pF	
CIO	Input/Output Capacitance (2)		8	10	pF	

Notes: (1) Except pins 6, 9
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 5.0V			
SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
tLX	LXMAR Pulse Width	230		ns	CL = 50pF
tAS	Address Setup Time	80		ns	See Timing Diagram
tAH	Address Hold Time	120		ns	
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$ $\overline{C2}$		190	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}$/$\overline{INT}$		210	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		250	ns	
tDS	Data Setup Time	30		ns	
tDH	Data Hold Time	120		ns	
tDPO	Delay: $\overline{DEVSEL}$ to Port Data		40	ns	
tPSLX	Port Data Setup LXMAR	30		ns	
tPHLX	Port Data Hold LXMAR	120		ns	
tPSIR	Port Data Setup IRS	20		ns	
tPHIR	Port Data Hold IRS	120		ns	
tPEN	Port B Enable Time		175	ns	
tPDIS	Port B Disable Time		175	ns	
tDR	Delay: IRS to IRE				
	ORS to ORF				
	$\overline{DEVSEL}$ to IRE				
	$\overline{DEVSEL}$ to ORF		340	ns	

Timing Diagram

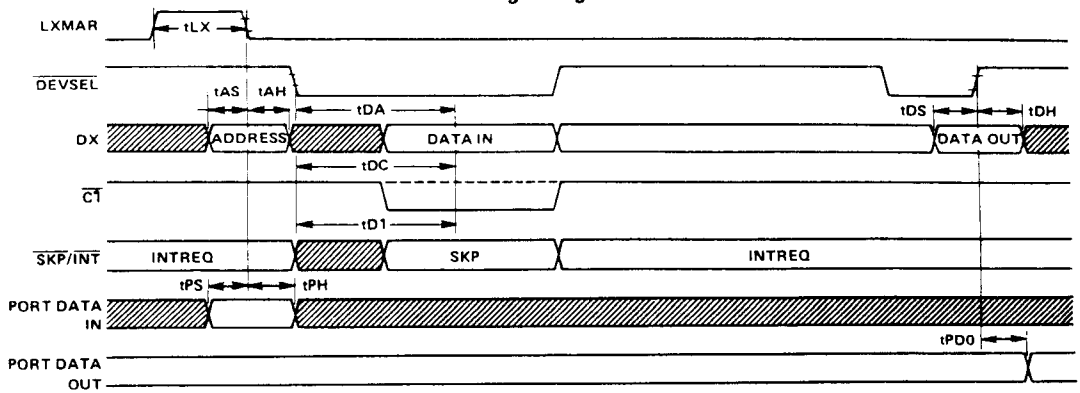


FIGURE 1-1 – HD-6103 PIO Timing Diagram

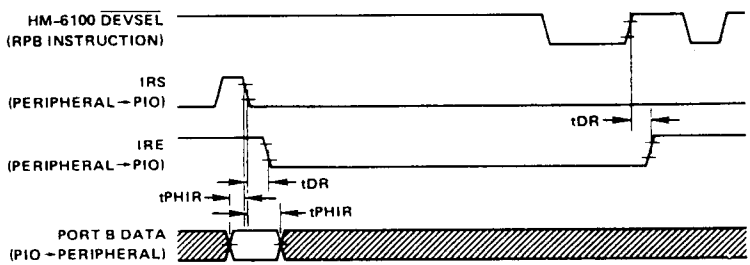


FIGURE 1-2 – Input Data Transfer (Peripheral device to PIO)

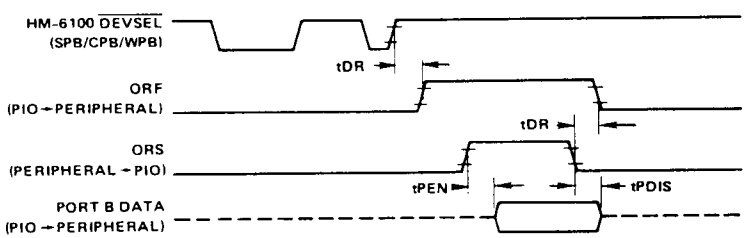


FIGURE 1-3 – Output Data Transfer (PIO to Peripheral device)

HD-6103 System Timing

The three-state bi-directional 12-bit DX bus is used to transfer data and control information (Fig. 3) between the HD-6103 and the HM-6100 microprocessor. The HM-6100 transmits the device address and control information on the DX bus during the 'execute' phase of an Input-Out put Transfer (IOT) instruction. The HD-6103 accepts this information on the falling edge of the LXMAR (Address Latch Enable) Signal.

The address bits (6-7) are compared with the chip select inputs (SEL6 and SEL7) to address 1 of 4 PIO's. The IOT address bits (3-5) are programmed internally to respond to the bit pattern 011. The SEL6 and SEL7 inputs should be externally hard-wired to match the DX6 and DX7 chip select bits. As shown in Fig. 3, $\overline{\text{DEVSEL}}$ goes low, during the first half of an IOT execute machine cycle for a read operation and it goes low again in the second half for a write operation. The HD-6103 responds to a 'read' instruction by putting data on the DX bus and $\overline{\text{C1}}$ output (of HM-6100) low when $\overline{\text{DEVSEL}}$ (from HM-6100) input is low. $\overline{\text{C1}}$ line goes low to indicate an input transfer cycle to the HM-6100. All PIO data transfers to the HM-6100 Accumulator (AC) is an 'OR' transfer, (i.e., PIO data is OR'ed into the contents of the AC).

During the write operation into PIO, the PIO accepts data from the HM-6100 Accumulator on the rising edge of the $\overline{DEVSEL}$. During and after the PIO write, the contents of the accumulator are not cleared.

$\overline{SKP/INT}$ line goes low during the 'read' $\overline{DEVSEL}$ if the HD-6103 is responding to a 'skip' instruction, and the 'skip' condition is met, therefore causing the HM-6100 to skip the next sequential instruction. $\overline{SKP/INT}$ line reflects the interrupt request status of the HM-6100 at all times except during the 'read' $\overline{DEVSEL}$. The $\overline{SKP/INT}$ line goes low if an active interrupt request is pending. During read $\overline{DEVSEL}$ mode, the $\overline{SKP/INT}$ indicates the current skip condition. The bits are interpretted as shown below:

Note: Both $\overline{CI}$ and $\overline{SKP/INT}$ are open drain outputs which are wire OR'd with outputs from other HM-6100 peripheral controllers.

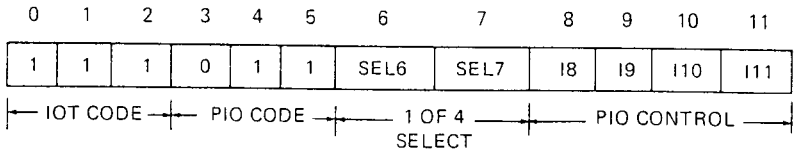


FIGURE 2 – PIO Instruction Format

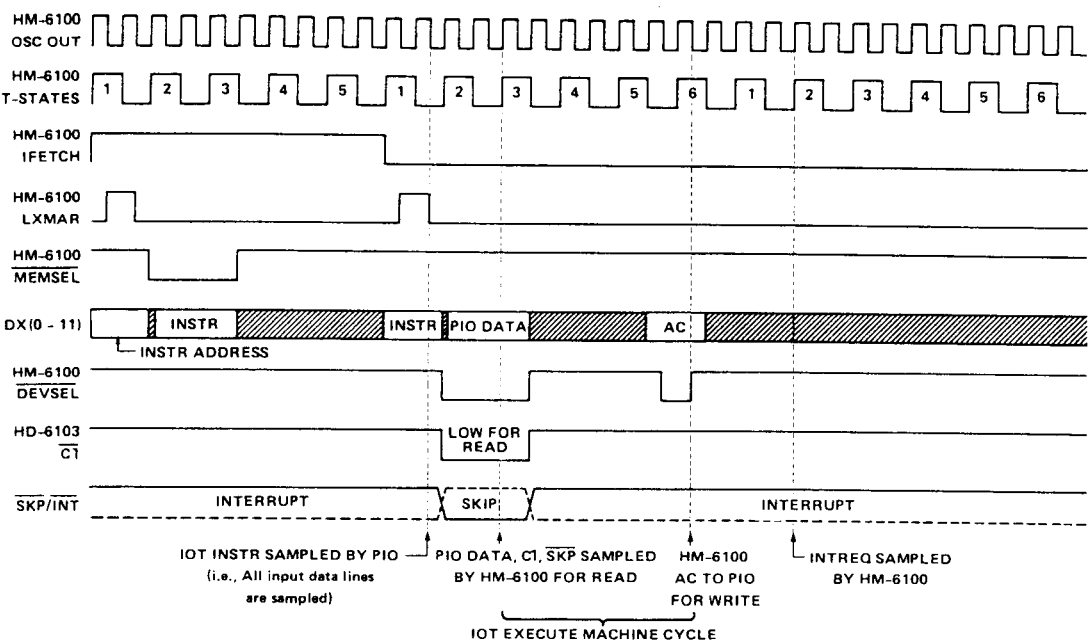


FIGURE 3 – HD-6103 System Timing Diagram

Operation of Port Buffers

The HD-6103 has 20 I/O pins which can be individually programmed in groups of 4, 8 or 12 bits in three different modes of operation.

In mode 11, the 20 I/O lines are divided into three ports:

- Port A with 4 bits (PA8 - PA11)
- Port B with 12 bits (PB0 - PB11)
- Port C with 4 bits (PC8 - PC11)

In mode 10, the 20 I/O lines are grouped into 2 ports:

- Port A with 8 bits (PA4 - PA11)
- Port B with 12 bits (PB0 - PB11)

The four I/O lines associated with Port C in Mode 11 (PC8 - PC11) are allocated to Port A as PA4 - PA7.

In mode 0X, there are two ports - Port B with 12 bits and Port C with 4 bits and four lines for handshake control logic. Four lines of Port A in Mode 11 (PA8 - PA11) are reassigned as handshake control lines. They are:

- Input Register Strobe (IRS)
- Input Register Empty (IRE)
- Output Register Strobe (ORS)
- Output Register Empty (ORE)

The handshake logic controls the data transfer for the Port B. Port C operation remains the same as in Mode 11.

For an 'input' transfer in 0X Mode, the input register empty (IRE) output goes high to indicate to the peripheral device that the input register is empty (as shown in Fig. 4).

The peripheral device may then strobe in the new data into Port B with Input Register Strobe (IRS). At this time, IRE goes low to indicate to the peripheral device that the input buffer is full, and remains low until Port B has been read by the HM-6100 microprocessor. IRE then goes high after the HM-6100 executes a Read Port B (RPB) instruction to initiate another input sequence. The data into Port B should be valid only for a short duration before and after IRS makes the 1 to 0 transition.

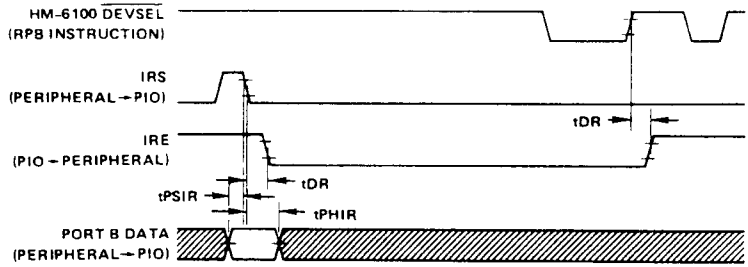


FIGURE 4 – Input Data Transfer (Peripheral device to PIO)

For an 'output' transfer in 0X mode, the HM–6100 microprocessor writes the data into Port B and its timing is shown in Fig. 5. ORF line from the PIO goes high, signaling the peripheral device that the output register is full. The peripheral device may then strobe in the new data from Port B with ORS. Port B stays in the high impedance mode until ORS is activated by the peripheral device. ORF line goes low and remains low until Port B has been written into by the HM-6100 microprocessor. ORF then goes high, initiating another output sequence.

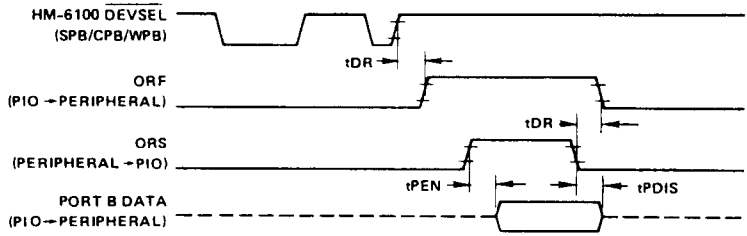


FIGURE 5 – Output Data Transfer (PIO to peripheral device)

The HM-6100 monitors the status of ORF (Output Register Full). If it is low (i.e., output register is empty), HM-6100 may load data into Port B output buffer with SPB/CPB/WPB instruction. ORF goes high a delay time after the rising edge of the 'write' $\overline{\text{DEVSEL}}$, signaling the peripheral device that output buffer has new data. During this time, Port B output buffers remain three-stated. The peripheral device may then enable and read out Port B output latches by activating ORS (Output Register Strobe) high. The falling edge of ORS (from high to low) signals the PIO that the peripheral device no longer needs the valid current information. Port B is three-stated and ORF then goes low, thereafter, to indicate another output sequence.

ORF should be set to 0 and IRE to 1 with a 'write' command in Mode 0X, to initiate the handshaking sequence.

The HM-6100 microprocessor should not write into Port B until ORF is low for an 'output' transfer and should not read Port B until IRE is low for an 'input' transfer. The peripheral device reads Port B if ORF is high and writes into Port B if IRE is high.

The PIO may be programmed to generate an $\overline{\text{INTREQ}}$ (Interrupt Request) to the microprocessor when ORF or IRE goes low by setting the respective Interrupt enable bits, OREN and IREN.

The HM-6100 may poll the status of ORF or IRE by executing the respective skip instructions SKPOR and SKPIR, by reading the status register or by reading "Port A".

In Mode 11 and 10, when handshaking control is not in effect, the execution of SKPOR and SKPIR Instructions depend on the state of the Port A lines PA11 and PA9, respectively. The Interrupt feature is available only in Mode 0X.

The mode of operation - 11, 10 or 0X, is selected by programming the Status Register (SR).

All ports are bi-directional. The execution of a 'write' instruction caused a port to be automatically programmed to be an 'output'. The output data may be changed by using the 'set', 'clear' or 'write' instructions. The output remains valid until the port bit lines are reset to be inputs.

Execution of a 'read' instruction causes a port to be automatically set as an 'input' port - i.e., it presents a very high impedance to the I/O lines. Data appearing on the I/O lines will be sampled into the port input latch at every LXMAR pulse and may be read by the HM-6100 microprocessor by the 'read' instruction.

In Mode 0X, Port B acts as a three-state bi-directional buffer which is controlled by an external peripheral device. ORF and IRE lines are outputs and ORS and IRS lines are inputs.

At power-on, all ports are defined to be input ports and the PIO is initialized to be in Mode 10. With 20 I/O lines partitioned into the 8/12 (i.e., Port A = 8 bits, Port B = 12 bits) format.

PIO Instructions

PIO CONTROL	MNEMONICS	DESCRIPTION
0000	SETPA	Set PA(i) to 1 if AC(i) is 1. AC is not cleared. Mode 11: PA(i) ← PA(i) + AC(i), $8 \leq i \leq 11$ Mode 10: PA(i) ← PA(i) + AC(i), $4 \leq i \leq 11$ Mode 0X: IREN ← IREN + AC(8) IRE ← IRE + AC(9) OREN ← OREN + AC(10) ORF ← ORF + AC(11)
0001	CLRPA	Clear Port A. Clear PA(i) to 0 if AC(i) is 1. AC is not cleared. Mode 11: PA(i) ← PA(i) ^ $\overline{AC(i)}$, $8 \leq 1 \leq 11$ Mode 10: PA(i) ← PA(i) ^ $\overline{AC(i)}$, $4 \leq i \leq 11$ Mode 0X: IREN ← IREN ^ $\overline{AC(8)}$ IRE ← IRE ^ $\overline{AC(9)}$ OREN ← IREN ^ $\overline{AC(10)}$ ORF ← ORF ^ $\overline{AC(11)}$
0010	WPA	Write Port A. Set PA(i) = AC(i). AC is not cleared. Mode 11: PA(i) ← AC(i), $8 \leq i \leq 11$ Mode 10: PA(i) ← AC(i), $4 \leq i \leq 11$ Mode 0X: IREN ← AC(8) IRE ← AC(9) OREN ← AC(10) ORF ← AC(11)
0011	RPA	Read Port A. 'OR' transfer PA to AC. Mode 11: AC(i) ← AC(i) + PA(i), $8 \leq i \leq 11$ AC(i) ← AC(i), $0 \leq i \leq 7$ Mode 10: AC(i) ← AC(i) + PA(i), $4 \leq i \leq 11$ AC(i) ← AC(i), $0 \leq i \leq 3$ Mode 0X: AC(8) ← AC(8) + IRS AC(9) ← AC(9) + IRE AC(10) ← AC(10) + ORS AC(11) ← AC(11) + ORF AC(i) ← AC(i), $0 \leq i \leq 7$
0100	SETPB	Set Port B. Set PB(i) to 1 if AC(i) is 1. AC is not cleared. PB(i) ← PB(i) + AC(i), $0 \leq i \leq 11$
0101	CLRPB	Clear Port B. Clear PB(i) to 0 if AC(i) is 1. AC is not cleared. PB(i) ← PB(i) ^ $\overline{AC(i)}$, $0 \leq i \leq 11$
0110	WPB	Write Port B. Set PB(i) = AC(i). AC is not cleared PB(i) ← AC(i), $0 \leq i \leq 11$
0111	RPB	Read Port B. 'OR' transfer PB to AC. AC(i) AC(i) + PB(i), $0 \leq i \leq 11$

PIO CONTROL	MNEMONICS	DESCRIPTION
1000	SETPC	Set Port C. Set PC(i) to 1 if AC(i) is 1. AC is not cleared. Mode 11 and 0X: PC(i) ← PC(i) + AC(i) $8 \leq i \leq 11$ Mode 10: No operation
1001	CLRPC	Clear Port C. Clear PC(i) to 0 if AC(i) is 1. AC is cleared. Mode 11 and 0X: PC(i) ← PC(i) ^ $\overline{AC(i)}$ $8 \leq i \leq 11$ Mode 10: No operation.
1010	WPC	Write Port C. Set PC(i)=AC(i). AC is not cleared Mode 11 and 0X: PC(i) ← AC(i) $8 \leq i \leq 11$ Mode 10: No operation.
1011	RPC	Read Port C. 'OR' transfer PC to AC. Mode 11 and 0X: AC(i) ← AC(i) + PC(i) $8 \leq i \leq 11$ Mode 10: No operation.
1100	SKPOR	Skip the next sequential instruction if PA(11))/ ORF is low. Mode 11 and 10: Skip if PA(11) is low. Mode 0X: Skip if ORF is low.
1101	SKPIR	Skip the next sequential instruction if PA(9)/ ORF is low. Mode 11 and 10: Skip if PA(9) is low. Mode 0X: Skip if IRE is low.
1110	WSR	Write status Register. AC is not cleared. M(8) ← AC(8) M(9) ← AC(9)
1111	RSR	Read Status Register. 'OR' transfer Status Register to AC. AC(i) ← AC(i), $0 \leq i \leq 7$ AC(8) ← AC(8) + M(8) AC(9) ← AC(9) + M(9) Mode 11 and 10: AC(10) ← AC(10) + PA(11) AC(11) ← AC(11) + PA(9) Mode 0X: AC(10) ← AC(10) + ORINT AC(11) ← AC(11) + IRINT

Symbol definition:
^ "and"
+ "or"
← "is replaced by"

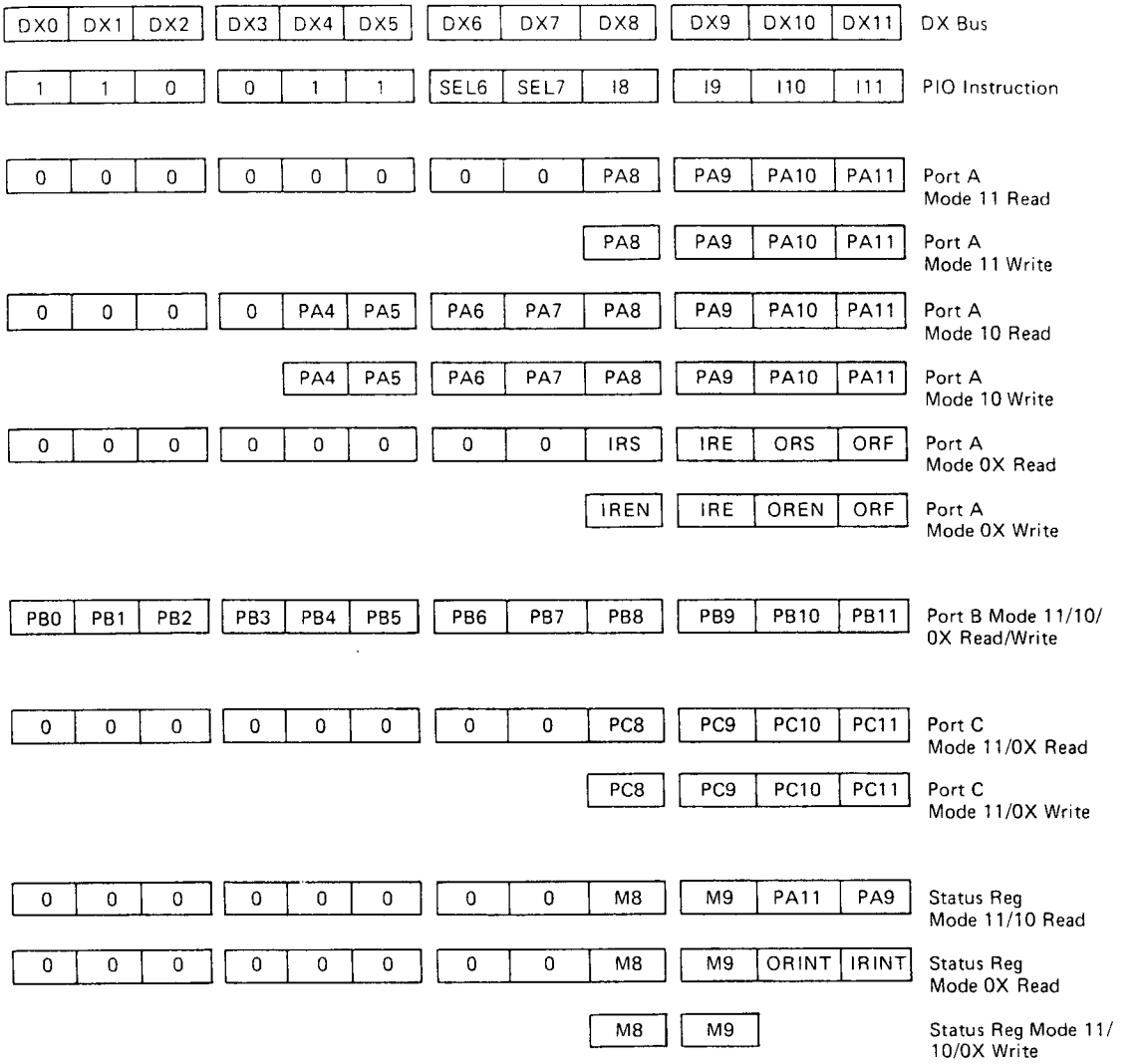


FIGURE 6 – HD-6103 PIO Register Bit Assignments

Pins	2	3	4	5	7	8	11	13	29	30	31	32	33	34	35	36	37	38	39	40
Mode 10	PA7	PA6	PA5	PA4	PA8	PA9	PA10	PA11	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB6	PB8	PB9	PB10	PB11
Mode 11	PC11	PC10	PC9	PC8	PA8	PA9	PA10	PA11	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7	PB8	PB9	PB10	PB11
Mode0X	PC11	PC10	PC9	PC8	IRS	IRE	ORS	ORF	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7	PB8	PB9	PB10	PB11

FIGURE 7 – HD-6103 PIO Port Pin Assignments

STATUS REGISTER

The Status Register (SR) has 2 mode bits, M8 and M9 which can be modified by the WSR (Write Status Register) instruction. These two bits define the mode of operation for the HD-6103 as shown in Figure 8.

M8	M9	MODE	PORT OPERATION
0	*	Mode 0X	PB(0)-(11), PC(8)-(11), IRS, IRE, ORS, ORF
1	0	Mode 10	PB(0)-(11), PA(4)-(11)
1	1	Mode 11	PB(0)-(11), PC(8)-(11), PA(8)-(11)

FIGURE 8 – Mode Bit Assignments

The Mode and Interrupt status bits, ORINT (Output Register empty Interrupt) and IRINT (Input Register empty Interrupt), may be read with the RSR (Read Status Register) instruction. The interrupt status bits are set to 0 if the corresponding flag is requesting an interrupt.

In Mode 11/10 the current value of PA11 and PA9 can be interrogated. In this mode, Port A can be either an input or an output. M(8) and M(9) are initialized to '11' at power-on.

MODE	COND-ITION	BIT ASSIGNMENTS			
		DX8	DX9	DX10	DX11
0X	READ	M8	M9	ORINT	IRINT
11/10	READ	M8	M9	PA11	PA9
11/10/0X	WRITE	M8	M9		

FIGURE 9 – Status Register Bit Assignments

SKIP OPERATION

The HM-6100 may poll the status of ORF or IRE in Mode 0X, by executing a skip instruction, SKPOR or SKPIR. The HD-6103 will assert the $\overline{SKP/INT}$ line low if the corresponding status line (ORF or IRE) is low, causing the next sequential instruction to be skipped. During this cycle, ORF and IRE remain unchanged.

In Mode 11/10, SKPOR and SKPIR instruction executions depend on the state of PA11 and PA9, respectively. Port A may be an input or output port.

If ORF is reset to 0 be executing a CLRPA or WPA instruction to initiate the handshaking sequence, the next SKPOR instruction will cause the next sequential instruction to be skipped.

INTERRUPT OPERATION

The HD-6103 may be programmed to generate an interrupt request input ($\overline{INTREQ}$) when ORF or IRE goes low, by setting the corresponding interrupt enable bits, OREN or IREN, to 1. If the HM-6100 interrupt system has been previously enabled, the microprocessor will acknowledge the $\overline{INTREQ}$ input. If the HM-6100 microprocessor does not see the higher priority $\overline{INTREQ}$'s, inputs from other peripheral controllers such as HD-6102 Memory Extender/Direct Memory Access/Internal Timer Controller (MEDIC) or HD-6101 Parallel Interface Elements (PIE) in the system, the interrupt service routine should initiate a software poll of the PIO's in the system to identify the particular PIO that generated the $\overline{INTREQ}$. In Mode 0X, the interrupt request status of ORF and IRE may be identified by reading the Status Register. ORINT or IRINT will be set to 0 if ORF (being low) or IRE (being low) is generating an $\overline{INTREQ}$. Note that HD-6102 MEDIC and HD-6101 PIE provide an automatic priority vectoring.

The interrupt feature of HD-6103 is available only in Mode 0X. An ORF $\overline{INTREQ}$ may be removed by one of the following methods:

- Executing an SPB/CPB/WPB Instruction (ORF goes high if Port B is written into), or
- Setting ORF to 1 with SPA/WPA Instruction, or
- By resetting OREN to 0 with a CPA/WPA Instruction, or
- By changing to Mode 11/10.

An IRE INTREQ may be removed by:

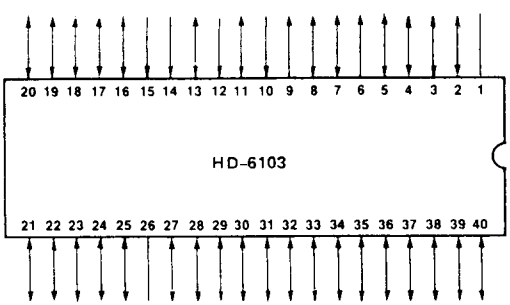
- Executing a RPB Instruction (IRE goes higher after Port B is read), or
- Setting IRE to 1 with SPA/WPA Instruction, or
- Resetting IREN to 0 with a CPA/WPA Instruction, or
- Changing to Mode 11/10.

PIO may be software programmed to generate an $\overline{INTREQ}$ to the HM-6100 by resetting ORF or IRE to 0 with a CPA/WPA Instruction and by setting the corresponding enable bit, OREN or IREN, with a SPA/WPA Instruction in Mode 0X.

PIN DEFINITIONS

PIN NO.	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
1	VCC		Positive Power Supply
2	PA7	I/O	Port A I/O Line (7)
	PC11	I/O	Port C I/O Line (11) in Mode 11/0X
3~5	PA6~PA4	I/O	Port A6~A4 (Mode 10).
	PC10~PC8	I/O	Port C10~C8 (Mode 11/0X).
6	$\overline{SKP}/\overline{INT}$	O	Time Multiplexed $\overline{SKP}$ and $\overline{INTREQ}$ lines to the HM-6100 Microprocessor – Active Low. This output is open drain.
7	PA8	I/O	Port A I/O Line in Mode 11/10 – Most Significant Bit of Port A in Mode 11.
	IRS	O	Input Register Strobe to clock data into Port B in Handshake Mode (Mode 0X). Port B Latches in the data on the falling edge of IRS (IRS↓).
8	PA9	I/O	Port A9 (Mode 11/10).

PIN NO.	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
8 Cont'd	IRE	O	Input Register Empty output goes high when Port B input buffer has been read by the HM-6100 Microprocessor. It goes low when Port B input buffers are strobed in by IRS↓. (Mode 0X). PIO may be programmed to generate an $\overline{INTREQ}$ on IRE↓.
9	$\overline{C1}$	O	C1 output goes low upon completion of PIO Port data transfer to the HM-6100 Accumulator (AC). This output is an open-drain output to be wire-OR'd with $\overline{C1}$ Lines from other HM-6100 peripheral controllers
10	LXMAR	I	Address Latch enable signal from the HM-6100. PIO clocks in address and control information from the HM-6100 on the falling edge of LXMAR (LXMAR↓). All Port inputs are sampled at LXMAR↓.



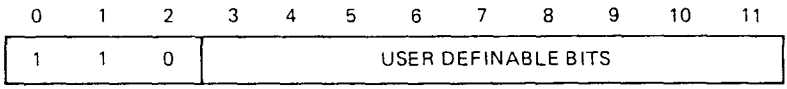
PIN NO.	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
11	PA10	I/O	Port A10 (Mode 11/10).
	ORS	I	Output Register Strobe input to Enable Port B output buffers in Mode 0X. Port B is three-stated when ORS is low.
12	$\overline{DEVSEL}$	I	Input-Output Device Select control line from the HM-6100. It performs both the read and write function. The first negative transition after LXMAR↓, enables the DX output buffer of the selected PIO for a read operation. When $\overline{DEVSEL}$ returns high, the 'read' operation is terminated. The second negative-going pulse on $\overline{DEVSEL}$ serves as a 'write' pulse to the selected PIO and the HM-6100 AC data is written into the selected PIO register or port on the rising edge.
13	PA11	I/O	Port A11 (Mode 11/10)-Least Significant bit of Port A.

PIN NO.	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
13 Cont'd	ORF	O	Output Register Full output goes high when the HM-6100 writes into Port B in a handshake mode. It goes low when the peripheral device reads Port B by enabling ORS high. The PIO may be programmed to generate an $\overline{INTREQ}$ on ORF↓ (Mode 0X).
14	SEL6	I	A Chip Select Input. PIO has 2 chip selects, SEL6 and SEL7, thereby enabling up to 4 PIO chips in a system.
15	SEL7	I	A Chip Select Input.
16~25	DX0~DX9	I/O	The HM-6100 System bus (Data and Address).
26	GND		Ground
27~28	DX10~DX11	I/O	HM-6100 System bus (Data and Address).
29~40	PB0~PB11	I/O	I/O Port Pin. PB0 is the most Significant bit, and PB11 is the Least Significant bit.

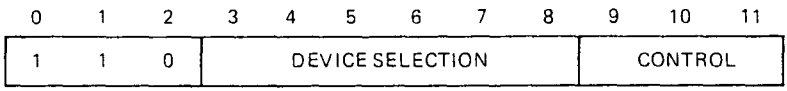
IOT Considerations

The HM-6100 communicates with peripherals via input/output transfers (IOT) instructions. The first three bits, 0-2 are always set to 68 (110) to specify an IOT instruction. The next 9 bits, 3-11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permits interfaces with up to 63 I/O devices. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The HD-6102 MEDIC utilizes the PDP-8/E format. When using the HD-6101 PIE and the HD-6103 PIO, bits 3-7 perform the device selection function and bits 8-11 provide the operation specification code.

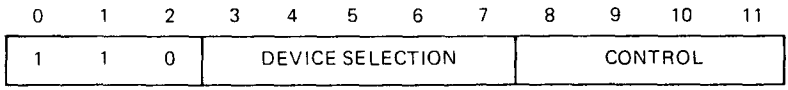
IOT INSTRUCTION FORMAT



Basic IOT Instruction: $6XXX_8$



PDP-8/E Format: $6NNX_8$



PIE and PIO Format

Care must be taken when building a system which uses all three peripheral interface devices from Harris to avoid conflicts with the device selection codes. Care also must be used when utilizing DEC compatible teletype and high speed reader interfaces in a system which includes PIE's and PIO's. The following table will assist in the assignment of device selection codes.

DEVICE SELECTION		DEVICE TYPE
PDP-8/E ①	PIE & PIO ②	
00	000 00	Internal IOT's
01	000 00	DEC High Speed Reader
02	000 01	DEC High Speed Punch
03	000 01	DEC Teletype Keyboard/Reader
04	000 10	DEC Teletype Printer/Punch
05	000 10	User Definable (DEC PDP-8/E Format Only)
06, 07	000 11	User Definable
10, 11	001 00	User Definable
12	001 01	User Definable (DEC PDP-8/E Format Only)
13	001 01	MEDIC Real Time Clock
14, 15	001 10	User Definable
16, 17	001 11	User Definable
20, 21	010 00	MEDIC Extended Memory Control and DMA
22, 23	010 01	MEDIC Extended Memory Control and DMA
24, 25	010 10	MEDIC Extended Memory Control and DMA
26, 27	010 11	MEDIC Extended Memory Control and DMA
30, 31	011 00	HD-6103 PIO No. One
32, 33	011 01	HD-6103 PIO No. Two
34, 35	011 10	HD-6103 PIO No. Three
36, 37	011 11	HD-6103 PIO No. Four
40, 41	100 00	User Definable
42, 43	100 01	
44, 45	100 10	
46, 47	100 11	
50, 51	101 00	
52, 53	101 01	
54, 55	101 10	
56, 57	101 11	
60, 61	110 00	
62, 63	110 01	
64, 65	110 10	
66, 67	110 11	(DEC Line Printer = 66)
70, 71	111 00	
72, 73	111 01	
74, 75	111 10	(DEC Floppy Disk Drive = 75)
76, 77	111 11	User Definable

NOTES:

① PDP-8/E device selection in octal.

② PIE & PIO device selection in binary.